Attorney Docket No.
MXICP012
(P910229)

PATENT APPLICATION

METHOD OF IMPROVING THERMAL STABILITY FOR COBALT SALICIDE

INVENTOR: Chin-Ta Su
No. 16, Li-Hsin Road, Science-Based Industrial Park
Hsinchu, Taiwan, R.O.C.
Citizenship: R.O.C.

ASSIGNEE: Macronix International Co., Ltd.

MARTINE & PENILLA, LLP
710 Lakeway Drive, Suite 170
Sunnyvale, California 94085
Telephone: (408) 749-6900

METHOD OF IMPROVING THERMAL STABILITY FOR COBALT SALICIDE

by Inventor:

Chin-Ta Su

BACKGROUND OF THE INVENTION

1. Field of the Invention

[0001] The present invention relates generally to semiconductor fabrication and, more particularly, to a method for forming cobalt salicide having improved thermal stability.

2. Description of the Related Art

[0002] In the field of semiconductor manufacturing, design innovation is constantly challenged by manufacturing implementation. Theoretical possibilities evolve into components, assemblies, and products only as fast as manufacturing limitations can be overcome.

[0003] By way of example, processor performance continues to improve as dimension decreases. A decrease in dimension of a processor leads to an increase in transistor density, which increases device speed due to, among other things, shorter carrier transit. The ever-shrinking scale of processor dimension, however, presents significant challenges including, by way of example, vertical scaling of junctions and gate dielectrics, and advanced interconnect to minimize RC delay.

[0004] As is known, polycide and silicided junctions are used at the gate and diffusion level to reduce parasitic resistance. The self-aligned silicide (also referred to as "salicide") on the gate and source/drain reduces parasitic resistance, but line width limitations challenge implementation in smaller and smaller features and devices. One type of salicide that has proven particularly effective has been cobalt salicide. Cobalt is regarded as a useful material in self-aligned salicide processing because of its low resistance and its silicon compatible lattice structure. Cobalt and

cobalt salicide ($CoSi_2$), however, can penetrate into the junction area, resulting in junction leakage, increase in contact resistance, and deteriorating transistor current drive. Generally, high temperatures are required for reacting cobalt and silicon, and a significant portion of the silicon substrate gets consumed in the process, causing the undesirable changes in the gate junction depth. Therefore, in conventional semiconductor manufacturing processes, cobalt salicide processing is typically only used in mid- and back-end processes to avoid process temperatures that are too high. In some conventional applications, a titanium (Ti) or a titanium nitride (TiN) layer is formed on the cobalt layer to avoid cobalt oxidation, but thermal stability remains a challenge.

[0005] In consideration of the foregoing, what is needed is a method of improving the thermal stability of cobalt salicide to enable use of desirable cobalt salicide processes in front-end processing.

SUMMARY OF THE INVENTION

[0006] Broadly speaking, the present invention fills this need by providing cobalt salicide having improved thermal stability. The present invention can be implemented in numerous ways, including as a process, an apparatus, a system, a device, or a method. Several embodiments of the present invention are described below.

[0007] In one embodiment, a method of improving the thermal stability for cobalt salicide is provided. In this method, a substrate having a silicon layer formed thereon is provided. A cobalt layer is formed over the silicon layer, and a TiN_x layer is formed over the cobalt layer. The method further includes performing a first thermal process to form a cobalt salicide layer over the silicon layer, and then removing a non-reactive cobalt layer. The TiN_x layer includes x atoms of nitrogen for each atom of titanium in a TiN_x molecule, and the value of x is greater than 0.9.

[0008] In another embodiment, a method of forming cobalt salicide is provided. As used herein, the phrase "cobalt salicide" refers to self-aligned cobalt silicide, i.e., cobalt silicide formed by a self-aligning process. The method includes forming a layer of silicon, forming a layer of cobalt over the layer of silicon, and forming a layer of TiN_x over the layer of cobalt, with the value of x being greater than 0.9. The method further includes performing a first thermal process to form a layer of cobalt salicide over the layer of silicon.

[0009] The advantages of the present invention over the prior art are numerous. One notable benefit and advantage of the invention is that in embodiments of the present invention, N atoms of the TiN_x layer diffuse into the cobalt salicide layer, and the N atoms suppress cobalt salicide grains from collecting together during the thermal processes. A higher x ratio of TiN_x, that is, a higher ratio of N_x atoms to Ti atoms in

each molecule of TiN_x, achieves better performance. Therefore, the thermal stability of the cobalt salicide can be improved. With an improved thermal stability of the cobalt salicide, the cobalt salicide process can be used in front-end fabrication processes.

[0010] Other advantages of the invention will become apparent from the following detailed description, taken in conjunction with the accompanying drawings, illustrating by way of example the principles of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

[0011] The accompanying drawings, which are incorporated in and constitute part of this specification, illustrate exemplary embodiments of the invention, and together with the description serve to explain the principles of the invention.

[0012] Figure 1 shows a cross section of a semiconductor substrate in the process of being fabricated in accordance with one embodiment of the present invention.

[0013] Figure 2 shows a cross section of the semiconductor substrate, formed of the semiconductor substrate illustrated in Figure 1, following a first thermal process, in accordance with one embodiment of the invention.

[0014] Figure 3 shows a cross section of a semiconductor substrate as formed by the removal of the non-reactive Co layer and the TiN_x layer in accordance with an embodiment of the present invention.

[0015] Figure 4 shows a flow chart diagram illustrating the method operations performed to improve the thermal stability for cobalt salicide, in accordance with one embodiment of the present invention.

[0016] Figure 5 illustrates a front-end process application of cobalt salicide formed in accordance with one embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

[0017] A method to improve the thermal stability of cobalt salicide is described. In one embodiment, the method includes formation of a TiN_x layer over a cobalt layer prior to the thermal process to form the cobalt salicide. N atoms diffuse into the cobalt resulting in an improved thermal stability and enabling front-end implementation of cobalt salicide processes. In the following description, numerous specific details are set forth in order to provide a thorough understanding of the present invention. It will be understood, however, to one skilled in the art, that the present invention may be practiced without some or all of these specific details. In other instances, well known process operations have not been described in detail to avoid obscuring the present invention unnecessarily.

[0018] As an overview, in one embodiment, a substrate having a silicon layer thereon is provided. A cobalt layer is formed on the silicon layer, and a TiN_x layer is formed on the cobalt layer. In one embodiment, the value of x is greater than 0.9. A thermal process is performed to form a cobalt salicide layer, and the non-reactive cobalt layer is removed.

[0019] Figure 1 shows a cross section of a semiconductor substrate 100 in the process of being fabricated in accordance with one embodiment of the present invention. As shown in Figure 1, the semiconductor substrate 100 includes a substrate layer 102. The substrate layer 102 includes any and all previously fabricated layers or levels and features of the semiconductor substrate 100. As is known, semiconductor devices such as transistors, memory cells, etc., are typically fabricated as multi-layer structures, many of which are often interconnected. As shown in Figure 1, the substrate layer 102 is representative of any and all previously fabricated multiple-layer structures.

[0020] A silicon (Si) layer 104 is deposited over the substrate layer 102. In one embodiment, the Si layer 104 provides a base layer or level in which source/drain regions, gate features, junctions, etc. are fabricated. In the illustrated embodiment, a cobalt (Co) layer 106 is deposited over the Si layer 104, and a TiN_x layer 108 is deposited over the Co layer 106.

[0021] In one embodiment, the TiN_x layer 108 is formed using a sputtering process, and the gas used in the sputtering process comprises N_2 and Ar. In one embodiment, the ratio of N_2 to Ar is approximately 3:1. Additionally, the thickness of the formed TiN_x layer 108 should not to be too thick, and is preferably set between about 25 angstroms and about 100 angstroms.

[0022] In one embodiment, a first thermal process is performed to form a cobalt salicide layer. During the first thermal process, N atoms of the TiN_x layer 108 diffuse into the Co layer 106. Because the TiN_x layer 108 is formed to a thickness of between about 25 angstroms and about 100 angstroms, a smaller amount of the Ti of the TiN_x layer 108 diffuses into the Si layer 104 to form $TiSi_x$. As is known, both the thermal stability and the resistance of $TiSi_x$ are poor.

[0023] Figure 2 shows a cross section of the semiconductor substrate 120, formed of the semiconductor substrate 100 illustrated in Figure 1, following a first thermal process, in accordance with one embodiment of the invention. In the illustrated embodiment, the substrate layer 102 remains essentially unchanged. The Si layer 104 thins during thermal processing, and the new $CoSi_x$ layer 110 is formed. The $CoSi_x$ layer 110 is described in greater detail below. Over the $CoSi_x$ layer 110 remains a layer of unreacted Co 106, and the TiN_x layer 108.

[0024] In one embodiment, a next process is performed, following the first thermal process described above, to remove the non-reactive Co layer 106 and the TiN_x layer

108. Figure 3 shows a cross section of a semiconductor substrate 130 as formed by the removal of the non-reactive Co layer 106 and the TiN_x layer 108 (see Figure 2) in accordance with an embodiment of the present invention. The resulting semiconductor substrate includes a substrate layer 102, an Si layer 104, and a $CoSi_x$ layer 110.

[0025] In one embodiment, a second thermal process is performed to enhance the conductivity of the cobalt salicide ($CoSi_x$) layer 110. In the second thermal process, the Co_2Si or CoSi formed during the first thermal processing would change to $CoSi_2$, and the resistance of the cobalt salicide would be decreased.

[0026] In embodiments of the present invention, nitrogen (N) atoms in the TiN_x layer 108 (see Figure 2) diffuse into the cobalt (Co) 106 and cobalt salicide ($CoSi_x$) layers 110 (see Figure 2). If N atoms of the TiN_x layer 108 were not permitted or induced to diffuse into the cobalt salicide ($CoSi_x$) layer 110, the cobalt salicide grains collect to form larger grains in initial and subsequent thermal processes. These larger grains do not connect together within the cobalt salicide layer, and the large, unconnected grains cause poor conductivity of the typically formed cobalt salicide layer.

[0027] In embodiments of the present invention, however, N atoms of the TiN_x layer 108 (see Figure 2) diffuse into the cobalt salicide layer 110 and suppress the cobalt salicide grains from collecting together. Therefore, the conductivity of the cobalt salicide formed in accordance with the principles described herein is improved.

[0028] Figure 4 shows a flow chart diagram 150 illustrating the method operations performed to improve the thermal stability for cobalt salicide, in accordance with one embodiment of the present invention. The method begins with operation 152 in which a substrate is provided. In one embodiment, the substrate has a silicon layer formed thereon. The substrate can be of any size and type compatible and useful for

typical operations in which cobalt salicide is an appropriate and useful feature. Typical substrate sizes include 200 mm and 300 mm silicon wafers used in semiconductor manufacturing, and additional sizes and materials used in the fabrication of flat panel display features, hard disk drive features, MEMS, etc. The silicon layer can be a first layer in the fabrication of features in the substrate, or the substrate can have from one to a plurality of layers of features or structures, being fabricated therein, and the silicon layer forms, in one embodiment, a base layer for the fabrication of a multi-layer structure on the substrate.

[0029] The method continues with operation 154 in which a cobalt layer is formed over the silicon layer. Embodiments of the present invention provide for improved thermal stability of cobalt salicide, and in operation 154, the cobalt layer to be silicided (or "salicided" in the case of a self-aligned process) is formed over the silicon layer.

[0030] Next, in operation 156, a TiN_x layer is formed over the cobalt layer. In one embodiment of the invention, the N atoms of the TiN_x layer will diffuse into the cobalt salicide layer formed during the first thermal processing described below. The N atoms suppress the cobalt salicide grains from collecting together during thermal processing, improving the thermal stability of the cobalt salicide.

[0031] The TiN_x layer is formed, in one embodiment, with the value of x being larger than 0.9. In one embodiment, the TiN_x layer is formed by a sputtering process. In a further embodiment, the sputtering process is accomplished with a gas consisting of N_2 and Ar. In one embodiment, the N_2 and the Ar in the sputtering gas are provided in concentrations at a ratio of approximately 3:1. In one embodiment, the TiN_x layer is formed to a thickness in a range of approximately 25 angstroms to approximately 100 angstroms.

[0032] The method continues with operation 158 in which a first thermal process is performed in the formation of cobalt salicide. The thermal process may be any known thermal process, however, in the present invention, the increased thermal stability of the cobalt results in formation of cobalt salicide without undesirable side effects such as substantial cobalt penetration into silicon and into gate/junction regions.

[0033] In operation 160, any non-reacted cobalt is removed. In one embodiment, once any non-reacted cobalt has been removed in operation 160, the method concludes with operation 162 in which a second thermal process is performed. In one embodiment, a second thermal process is performed as shown in operation 162 to enhance the conductivity of the cobalt salicide layer. In the second thermal process, Co_2Si or CoSi are converted to $CoSi_2$, and the resistance of the cobalt salicide is decreased.

[0034] Embodiments of the present invention provide for improved thermal stability of cobalt salicide. In contrast with the conventional formation of cobalt salicide in which process temperatures are so high as to decrease the conductivity of the cobalt salicide and dictate only mid- and back-end process applications, the cobalt salicide layer in embodiments of the present invention can be used in the front-end process, such as applying self-aligned cobalt silicide, i.e., cobalt salicide, on the buried source and drain of memory structures. In more detail, the cobalt salicide layer can be formed on the buried source and drain to improve the resistance.

[0035] Figure 5 illustrates a front-end process application of cobalt salicide formed in accordance with one embodiment of the present invention. In Figure 5, a cobalt salicided feature 170 is shown. In a substrate 172, a buried source and drain (BD) 174 has been formed. The substrate 172 can be an initial layer of a semiconductor wafer,

or the substrate 172 can be a layer over one or more fabricated features of multi-layer structures. Typically, the layer over one or more fabricated features of a multi-layer structure is fabricated of silicon or any other desired inter-layer dielectric material. A gate feature 176 is shown fabricated over and adjacent to the buried source and drain 174, and cobalt salicide 178 is shown formed over the buried source and drain 174 to improve the resistance of the junction.

[0036] In summary, the present invention provides a method for increasing the thermal stability of cobalt salicide during the formation of cobalt salicide in a plurality of applications. The invention has been described herein in terms of several exemplary embodiments. Other embodiments of the invention will be apparent to those skilled in the art from consideration of the specification and practice of the invention. The embodiments and preferred features described above should be considered exemplary, with the scope of the invention being defined by the appended claims and their equivalents.

What is claimed is: